วงจรเรียงกระแสแบบครึ่งคลื่นย่านความถี่สูงที่ใช้เทคนิคการทำงานในโหมดกระแส

อดิศักดิ์ มนต์ประภัสสร [1]
มหาวิทยาลัยเอเชียอาคเนย์ หนองแขม กรุงเทพฯ 10160

บทคัดย่อ

บทความนี้นำเสนอ วงจรเรียงกระแสแบบครึ่งคลื่นความถี่สูงที่มีโครงสร้างแบบซีมอส ซึ่งใช้เทคนิคของการทำงานในโหมดกระแส โดยวงจรที่นำเสนอมีย่านการตอบสนองความถี่สูงถึง 100 MHz วงจรที่นำเสนอนี้ประกอบด้วยส่วนประกอบหลัก 3 ส่วนคือ 1) วงจรเปลี่ยนแรงดันเป็นกระแสแบบใหม่ ซึ่งประกอบด้วยมอสเฟท 2 ตัว และแหล่งจ่ายกระแสคงที่ 2 ตัว 2) วงจรเรียงกระแสแบบครึ่งคลื่นโหมดกระแสที่ถูกดัดแปลงมาจากวงจรสะท้อนกระแสคลาส AB โดย (Kawahito and Tadokoro (1996), [1]) ซึ่งประกอบด้วยมอสเฟท 6 ตัว และแหล่งจ่ายกระแสคงที่ 2 ตัว และ 3) วงจรเปลี่ยนกระแสเป็นแรงดัน 2 วงจร ซึ่งประกอบด้วยตัวต้านทาน 2 ตัว นอกจากนี้ในงานวิจัยชิ้นนี้ยังได้นำเทคโนโลยีใหม่ของมอสเฟทขนาด 0.8 μm มาใช้ด้วย

ในส่วนของการทดลอง วงจรที่ออกแบบจะถูกเลียนแบบการทำงานโดยใช้โปรแกรม PSPICE ผลที่ได้จากการเลียนแบบการทำงานคือ วงจรที่ออกแบบมีย่านการตอบสนองความถี่ที่สูง ใช้อุปกรณ์น้อยและกำลังงานสิ้นเปลืองต่ำ วงจรเรียงกระแสที่นำเสนอมีเอาต์พุต 2 เอาต์พุต คือ เอาต์พุตของการเรียงกระแสครึ่งคลื่นแบบบวก และเอาต์พุตของการเรียงกระแสครึ่งคลื่นแบบลบ

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[1] *อาจารย์ประจำ สาขาวิชาวิศวกรรมอิเล็กทรอนิกส์ คณะวิศวกรรมศาสตร์*

High Frequency Half–wave Rectifier Based on Current Mode Technique

Adisak Monpapassorn [1]

South–East Asia University Nong–Kham Bangkok 10160

Abstract

This paper presents a CMOS high frequency half–wave rectifier based on current mode technique, which has a capacity for the frequency response up to 100 MHz. This circuit consists of three main components: 1) a new voltage to current circuit (V–I) is composed of two MOSFETs and two constant current sources; 2) a current mode half–wave rectifier that is applied from a class–AB current mirror circuit given by Kawahito and Tadokoro. This circuit is composed of six MOSFETs and two constant current sources; and 3) two current to voltage circuits (I–V) are composed of two resistors. In addition, the new 0.8 μm MOSFET technology has been applied in this research project.

In one experiment, the design circuit was simulated using the PSPICE program. The most important results reveal that the proposed circuit design provides high frequency response through employing low–level environments, both devices and power consumption. Two outputs of the proposed rectifier circuit are a positive and a negative half–wave rectifier outputs.

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[1] Lecturer, Department of Electronic Engineering, Faculty of Engineering

Introduction

The rectifier circuits are widely used in wattmeters, AC voltmeters, RF demodulators, piecewise linear function generators, and various nonlinear analog signal–processing circuits. The operation of only diode rectifiers are limited by the threshold voltages, approximately **0.3 V** for germanium diode and 0.7 **V** for silicon diode, thus they are used in only some applications of which the precision in range of threshold voltage is insignificant, such as radio frequency demodulators and DC voltage supply rectifiers. Nevertheless for the applications requiring high accuracy, the diode rectifiers cannot be used to treat the purpose. This problem can be solved using MOS or bipolar transistor integrated circuit rectifier instead, for example the rectifiers proposed in [2-7].

This paper proposes the new half–wave voltage rectifier using CMOS technology with unity voltage gain, moreover, the 0.8 μm MOSFETs are applied, thus it has an operating frequency higher than the above researches.

Proposed Circuit

A block diagram of the proposed circuit is shown in Fig. 1. The AC input voltage is converted to the AC input current by V–I, and this AC input current is rectified to a positive and a negative half–wave current signals by the current mode positive and negative half–wave rectifiers, respectively. Subsequently, these positive and negative half–wave current signals are converted to positive and negative half–wave output voltage signals by the first and the second load–resistors, respectively.

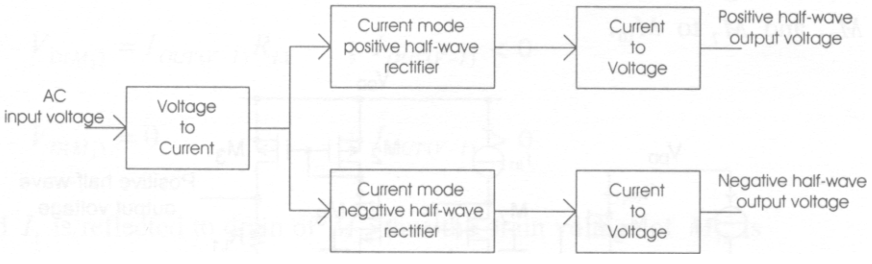


Fig. 1 Basic elements of the proposed half-wave rectifier.

1 New V–I

The **V–I** shown in Fig. **2** is composed of M_1, M,, I,, **,** and I,, **.** M_1 and M, are biased in saturation region. A source current of M_1 is

$$I_{S(M1)} = \beta_1 \left(V_{DD} - \left|V_{TP}\right| - V_{IN}\right)^2 \tag{1}$$

where

$$\beta_1 = K_P \frac{W_{M1}}{2L_{M1}}$$

and a drain current of M_6 is

$$I_{D(M6)} = \beta_6 \left(V_{IN} - V_{SS} - |V_{TN}|\right)^2 \qquad (2)$$

where

$$\beta_6 = K_N \frac{W_{M6}}{2L_{M6}}$$

Let $\beta_1 = \beta_6 = \beta$ by adjusting W_{M1}/L_{M1} and W_{M6}/L_{M6}, and let $|V_{TN}| = |V_{TP}| = V_T$ because they are almost the same values, the output current of the proposed V-I can be expressed as

$$I_{OUT(V-I)} = I_{S(M1)} - I_{D(M6)} + I_{B1} - I_{B2}$$

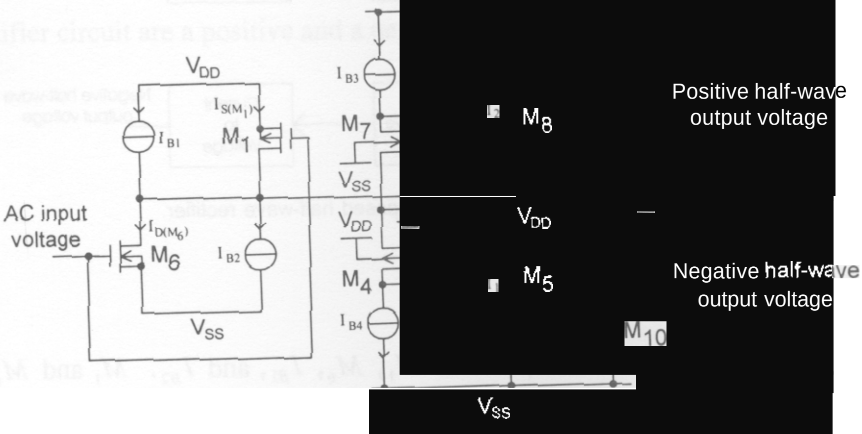
[redacted]

By employing I„ = I„ and $V_{DD} = -V_{SS}$, from $(a+b)^2 - (a-b)^2 = 4ab$, the output current can be written as

IO,(V-,j $= -4V_{IN}(V_{DD} - V_T)\beta$ (3)

2 Current mode half-wave rectifier and I-V

A proposed current mode half-wave rectifier circuit is applied from a class-AB current mirror circuit [1]. The proposed current mode rectifier circuit shown in Fig. 2, is composed of I_{B3}, I_{B4}, M_2 to M_5, and M_7 to M_{10}.



[redacted]

Fig. 2 The proposed half-wave rectifier circuit.

From the proposed current mode half–wave rectifier circuit, the input current of the circuit $(I_{OUT(V-I)})$ is separated into **two** current mirrors : the NMOS current mirror and the PMOS current mirror. M_8 and M_5 are also biased by M_7, M,, I,, and I_{B4}. The biased currents are set to I,, = I_{B4} = I,. If the drain conductance coefficients and the absolute values of the threshold voltage are the same for M_8 and M_5, the current components, I, and I, in Fig. 2, **[1]**given by

$$I_1 = \left(\frac{4I_B - I_{OUT(V-I)}}{4\sqrt{I_B}} \right)^2 \qquad (4)$$

$$I_2 = \left(\frac{4I_B + I_{OUT(V-I)}}{4\sqrt{I_B}} \right)^2 \qquad (5)$$

for $-41, \le I_{OUT(V-I)} \le 4I_B$. But, if $I_{OUT(V-I)} < -4I_B$, thus I, =I„„„ and I, = 0 ; and if $I_{OUT(V-I)} > 4I_B$, thus I, = $I_{OUT(V-I)}$ and I, = 0. By using the low value of I,, the relation of the currents in the circuit can be estimated **as**

for $I_{OUT(V-I)} > 0$,

$$I_1 = I_{„„} \quad \text{and} \quad I, = 0 \qquad (6)$$

and for $I_{OUT(V-I)} < 0$,

$$I, = I_{OUT(V-I)} \quad \text{and} \quad I, = 0 \qquad (7)$$

From Fig. **1,** I, is reflected to drain of M, thus the drain voltage of M, is

$$V_{D(M_3)} = I_{OUT(V-I)} R_{L1} \quad ; \; I_{OUT(V-I)} < 0 \qquad (8a)$$

$$V_{D(M_3)} = 0 \quad ; \; I_{OUT(V-I)} > 0 \qquad (8b)$$

and I, is reflected to drain of M_{10} thus the drain voltage of M_{10} is

$$V_{D(M_{10})} = I_{OUT(V-I)} R_{L2} \quad ; \; I_{OUT(V-I)} > 0 \qquad (9a)$$

$$V_{D(M_{10})} = 0 \quad ; \; I_{OUT(V-I)} < 0 \qquad (9b)$$

From the equations (8a), (8b), (9a), and 9(b); $V_{D(M_3)}$ and $V_{D(M_{10})}$ are the positive and the negative half–wave voltages of the **AC** input voltage, respectively. The unity voltage gain of the proposed rectifier circuit can be received by adjusting the load–resistor values.

Simulated Results

The proposed half-wave rectifier circuit was simulated by using the PSPICE program. Two DC power supplies are V_{DD} = +3VDC and *Vss* = –3VDC. Four constant current sources are *I*,, = *I*,, = 10 μA and *I*,, = I_{B4} = 0.1 μA. The W/L parameters of *M*, is 2.7 μm / 0.8 μm; M_6 is 1.1 μm / **0.8** μm; M_2- M_5 and M_7- M_{10} are 10 μm / 0.8 μm, using a SPICE model of the 0.8 μm MOSFET technology [8]. The values of *R*,, and R_{L2} are 5.7 KR and 6.9 KR, respectively. The positive **and** negative half–wave output signals of the circuit when the sine wave (10 **kHz,** 2V_{P-P}) is fed to the input, are shown in Fig. 3 and Fig. 4, respectively. And the positive and negative half–wave output signals of the circuit when the sine wave (100 MHz, 2V_{P-P}) is fed to the input, are shown in Fig. 5 and Fig. 6, respectively. The distortion of the output signals in Fig. 3, Fig. 4, Fig. 5, and Fig.6 comparing with the ideal half–wave signals are 1.9%, 4.9%, 6.7%, and 9.4%, respectively.

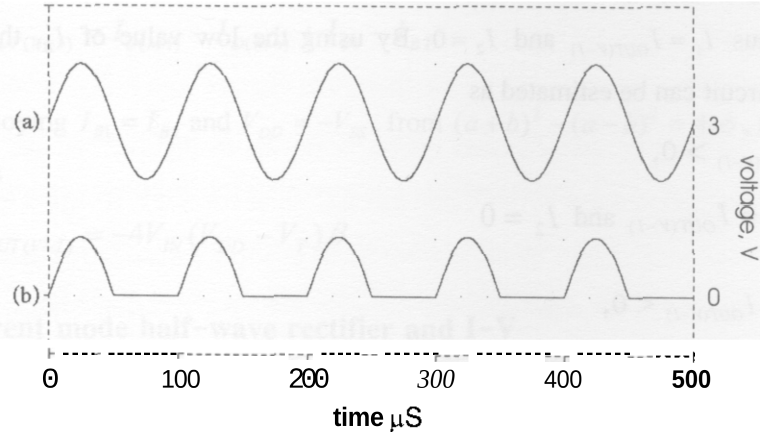


Fig. 3 **(a) the sine wave input signal** (10 **kHz. 2Vp-p) with the** DC **offset voltage** 3V
(b) the positive half-wave output signal

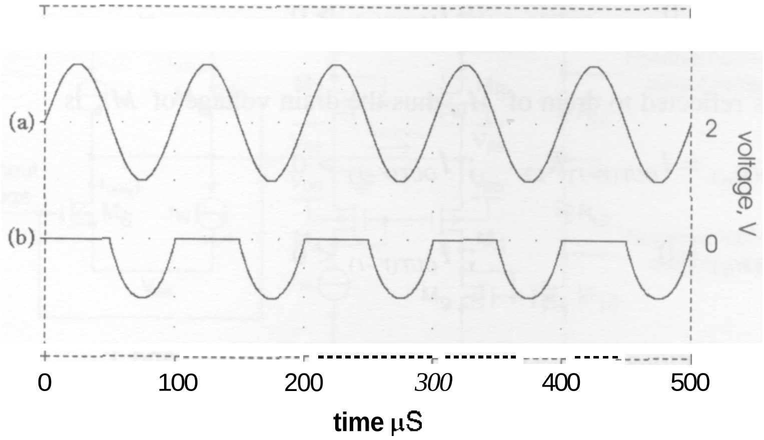


Fig. 4 **(a) the sine wave input signal** (10 **kHz.2Vp.p) with the** DC **offset voltage** 2V
(b) the negative half-wave output signal

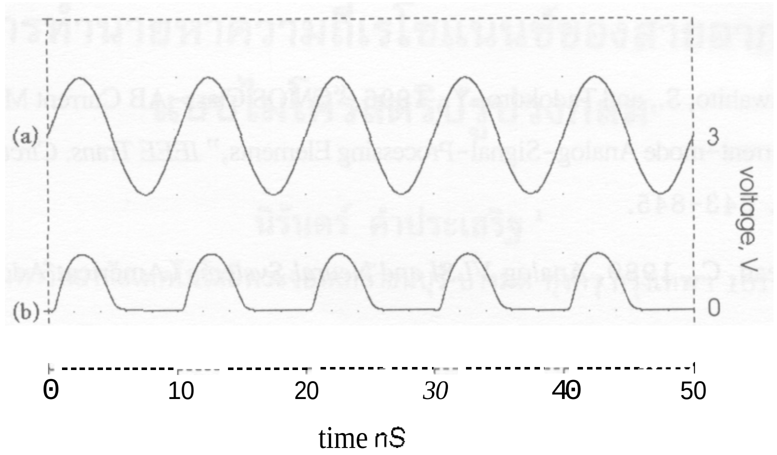


Fig. 5 (a) the sine wave input signal (100 **MHz,** 2Vp-p)with the DC offset voltage 3V

(b) the positive half-wave output signal

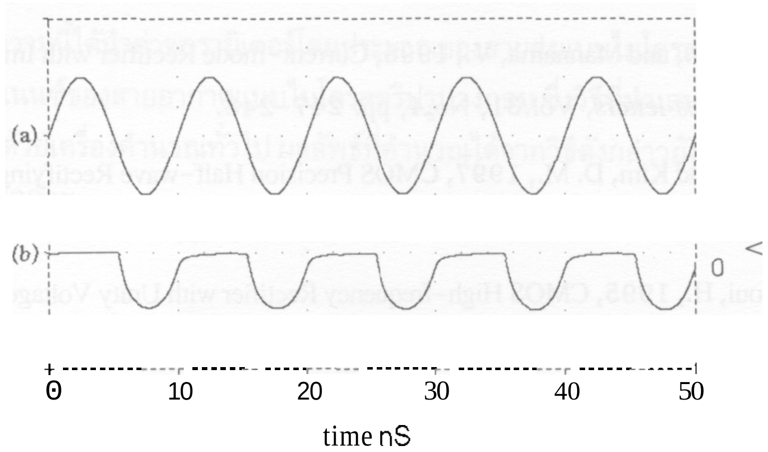


Fig. 6 (a) the sine wave input signal (100 MHz, 2Vp-p) with the DC offset voltage 2V

(b) the negative half-wave output signal

Conclusion

The advantages of this proposed half-wave rectifier are employing few numbers of components, low ship area, low voltage operation, and low power consumption to produce a operating frequency higher than one obtained from the other rectifiers in the references. This proposed circuit is suitable for the use in electronic and telecommunication applications.

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