การสร้างวงจรเรียงกระแสหลายหน้าที่โดยใช้วงจรสายพานกระแส

อดิศักดิ์ มนต์ประภัสสร[1] และ เสน่ห์ ไมตรีจิตร์[1]

มหาวิทยาลัยเอเชียอาคเนย์ หนองแขม กรุงเทพฯ 10160

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บทคัดย่อ

บทความนี้เสนอการสร้างวงจรเรียงกระแสหลายหน้าที่โดยใช้วงจรสายพานกระแส (CCII) 4 ชุด วงจรสายพานกระแส 4 ชุดนี้แบ่งแยกเป็น CCII+2 ชุด และ CCII+/-2 ชุด วงจรเรียงกระแสหลายหน้าที่ที่นำเสนอนี้สามารถทำการเรียงกระแสเป็นวงจรเรียงกระแสแบบครึ่งคลื่นบวก วงจรเรียงกระแสแบบครึ่งคลื่นลบ วงจรเรียงกระแสแบบเต็มคลื่นบวก และวงจรเรียงกระแสแบบเต็มคลื่นลบ ผลของการเลียนแบบการทำงานของวงจรโดยใช้โปรแกรม PSPICE ด้วยวงจรสายพานกระแสแบบ CMOS ที่ถูกสร้างด้วยเทคโนโลยี 0.5 μm ของ MIETEC แสดงให้เห็นว่าวงจรเรียงกระแสหลายหน้าที่ที่นำเสนอสามารถทำงานในย่านแรงดันอินพุตจาก -300 มิลลิโวลต์ ถึง 300 มิลลิโวลต์ ด้วยแรงดันแหล่งจ่ายเพียง ±1.2 โวลต์ และกำลังงานสิ้นเปลืองเพียง 0.88 mW ยิ่งไปกว่านั้น ผลการทดลองด้วยโปรแกรม PSPICE ยังแสดงให้เห็นถึงการเรียงกระแสสัญญาณไซน์ขนาด 100 mVpeak ความถี่ 100 กิโลเฮิรตซ์ ด้วย

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[1] *ผู้ช่วยศาสตราจารย์ สาขาวิชาวิศวกรรมอิเล็กทรอนิกส์*

Universal Rectifier Using Current Conveyors

Adisak Monpapassorn[1] and Sanae Maitreechit[1]

South-East Asia University, Nong-Kham, Bangkok 10160

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Abstract

A universal rectifier using four current conveyors, two second-generation current conveyors (CCII+s), and two CCII+/-s, is presented. The proposed rectifier performs positive half-wave, negative half-wave, positive full-wave and negative full-wave rectification in one circuit. Simulation results using the PSPICE program with CMOS current conveyors fabricated in 0.5 μm CMOS technology of MIETEC were performed. The results show that the proposed rectifier can be operated with an input voltage in the range of - 300 mV to 300 mV with the supply voltages of ±1.2 V and the power consumption of 0.88 mW. Additionally, the results also show the rectification for a 100 mVpeak sine wave signal at a frequency of 100 kHz.

[1] *Assistant Professor, Department of Electronic Engineering.*

1. Introduction

In small signal rectification, a simple diode rectifier cannot be used because of a limit of the threshold voltage, in the range of 0.2 V to 0.3 V for a germanium diode and 0.6 V to 0.7 V for a silicon diode. The combination of diodes with the active elements such as opamps, operational transconductance amplifiers, current conveyors, is a choice to make that the diode can rectify the voltage to be lower than the threshold voltage. Recently, a current conveyor rectifier has received widely attention. For example, LTP Electronics Ltd. [1] proposed the current conveyor positive half-wave and full-wave rectifiers. Toumazou *et al.* [2], Hayatleh *et al.* [3], Khan *et al.* [4] and Monpapassorn *et al.* [5] proposed the current conveyor positive full-wave rectifiers. In fact, all rectification of a single-phase signal is used in analog signal processing applications. Moreover, nowadays, the IC fabrication technology can integrate many transistors on one chip. Therefore, it is easy to create a large circuit on the chip. From all of the above, it will be convenient for applications if the rectifier can rectify the signal in every rectification.

In this paper, the authors present the combination of all rectification of the single-phase signal in a universal rectifier that uses two CCII+s, two CCII+/-s, four diodes and six resistors. While the positive full-wave rectifiers proposed by Toumazou *et al.* [2], Hayatleh *et al.* [3] and Khan *et al.* [4] use two CCII+, four diodes and two resistors. Additionally, the positive full-wave rectifier presented by Monpapassorn *et al.* [5] uses a CCII+, two resistors and four current mirrors. Comparing the proposed universal rectifier with the rectifiers proposed previously, we find that with minor adjusting the proposed rectifier can universally operate. More details of the proposed rectifier will be explained in the next sections.

2. Proposed Universal Rectifier

Sedra and Smith [6] introduced a second-generation current conveyor (CCII). Both CCII+ and CCII+/- in Fig. 1 are used in a proposed universal rectifier. The voltage and current transfer characteristics of the CCII+ is given by

$$\left.\begin{aligned} i_y &= 0 \\ v_x &= v_y \\ i_z &= i_x \end{aligned}\right\} \qquad \textbf{(1)}$$

and the transfer characteristics of the CCII+/- is given by

$$\left.\begin{aligned} i_y &= 0 \\ v_x &= v_y \\ i_{z+} &= i_x \\ i_{z-} &= -i_x \end{aligned}\right\} \qquad \textbf{(2)}$$

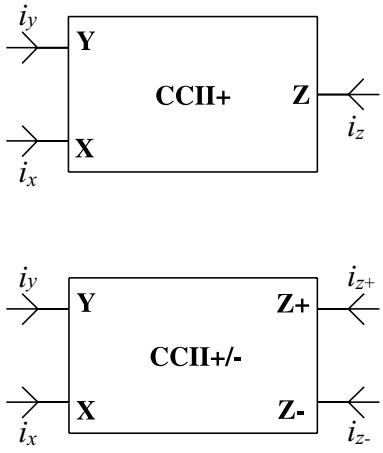


Fig. 1 Second generation current conveyors: CCII+ and CCII+/-.

The proposed universal rectifier is shown in Fig. 2. It consists of two CCII+s, two CCII+/-s, four diodes, and six resistors. Its operation is as follows. An input voltage (V_{in}) is applied to nodes Y of CCII+1 and CCII+2. Using Eq. 1, the currents at nodes Z and X of CCII+1 and CCII+2 can be written as

$$i_{z1} = i_{x1} = \frac{V_{in}}{R_1} \qquad \textbf{(3a)}$$

$$i_{z2} = i_{x2} = \frac{V_{in}}{R_2} \qquad \textbf{(3b)}$$

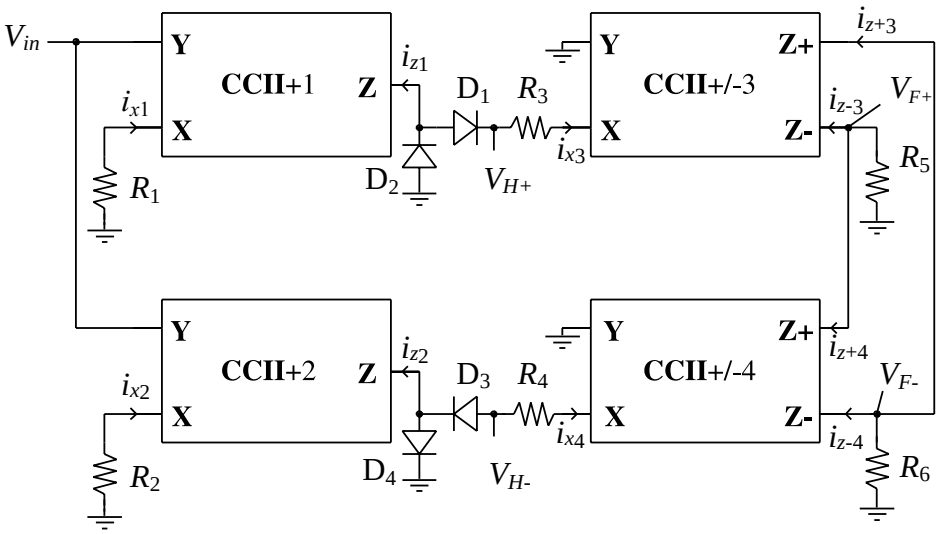


Fig. 2 Proposed universal rectifier.

The current i_{z1} is fed to the rectifier diodes, D_1 and D_2, and the current i_{z2} is fed to the rectifier diodes, D_3 and D_4. These diodes alternate between conduct and non-conduct to rectify the input voltage in the form of i_{z1} and i_{z2}. When the input voltage is positive; D_1 turned on and D_2 turned off, hence, i_{x3} is -i_{z1}; moreover, D_3 turned off and D_4 turned on, thus, i_{z2} is bypassed to ground, there is no i_{x4}. When the input voltage is negative; D_1 turned off and D_2 turned on, therefore, i_{z1} is bypassed to ground, having no i_{x3}; in addition, D_3 turned on and D_4 turned off, consequently, i_{x4} is -i_{x2}. Note that nodes Y of CCII+/-3 and CCII+/-4 are grounded, exploiting Eq. 2 in case $v_x = v_y$ and Eq. 3 as well as using $R_1 = R_2 = R_3 = R_4$, we can write the relations between the input voltage and the voltages V_{H+} and V_{H-} as

$$\left.\begin{array}{l} V_{in} > 0;\ V_{H+} = V_{in} \\ V_{in} < 0;\ V_{H+} = 0 \end{array}\right\} \quad \textbf{(4)}$$

and

$$\left.\begin{array}{l} V_{in} > 0;\ V_{H-} = 0 \\ V_{in} < 0;\ V_{H-} = V_{in} \end{array}\right\} \quad \textbf{(5)}$$

These mean that V_{H+} and V_{H-} are the positive and negative half-wave voltages, respectively.

Using Eq. 2 in case $i_{z+} = i_x$ and $i_{z-} = -i_x$ as well as $R_1 = R_2 = R_5 = R_6$, The relations between the input voltage and the voltages V_{F+} and V_{F-} can be expressed as

$$\left.\begin{array}{l} V_{in} > 0;\ V_{F+} = V_{in} \\ V_{in} < 0;\ V_{F+} = -V_{in} \end{array}\right\} \quad \textbf{(6)}$$

and

$$\left.\begin{array}{l} V_{in} > 0;\ V_{F-} = -V_{in} \\ V_{in} < 0;\ V_{F-} = V_{in} \end{array}\right\} \quad \textbf{(7)}$$

it is evident in Eq. 6 and Eq. 7 that V_{F+} and V_{F-} are the positive and negative full-wave voltages.

The values of resistors in the proposed rectifier affect the power consumption of the proposed rectifier. That is, if ones choose the low values of resistors resulting in the high currents in the rectifier, which are the cause of high power consumption. Hence, if the low power consumption is needed, the high values of resisters must be chosen. However, the use of high value resistors leads to the use of a wide chip area in an IC process.

In the above analysis, the resistance at nodes X of all CCIIs [6] is neglected, i.e., it is $0\ \Omega$. Practically, it affects the operation of the proposed rectifier. Namely the real i_{x1} and i_{x2}(i_{x1}* and i_{x2}*) are

$$i_{x1}^* = \frac{V_{in}}{R_1 + r_{x1}} \quad \textbf{(8a)}$$

$$i_{x2}^* = \frac{V_{in}}{R_2 + r_{x2}} \quad \textbf{(8b)}$$

where r_{x1} and r_{x2} are the resistance at nodes X of CCII+1 and CCII+2.

These currents are rectified and then are converted to voltages by $R_3 + r_{x3}$ for i_{x1}* and by $R_4 + r_{x4}$ for i_{x2}*. Therefore, the positive and negative half-wave voltages are true according to Eq. 4 and Eq. 5, where $r_{x1} = r_{x2} = r_{x3} = r_{x4} = r_x$ because the same input structure CCIIs are used. But, for the positive and negative full-wave voltages, only R_5 and R_6 convert output currents to voltages. Thus, the positive and negative full-wave voltages will be lower than Eq. 6 and Eq. 7. To solve this error, if $R_1 = R_2 = R_3 = R_4 = R$, R_5 and R_6 have to be set to

$$R_5 = R + r_x \quad \textbf{(9a)}$$

$$R_6 = R + r_x \quad \textbf{(9b)}$$

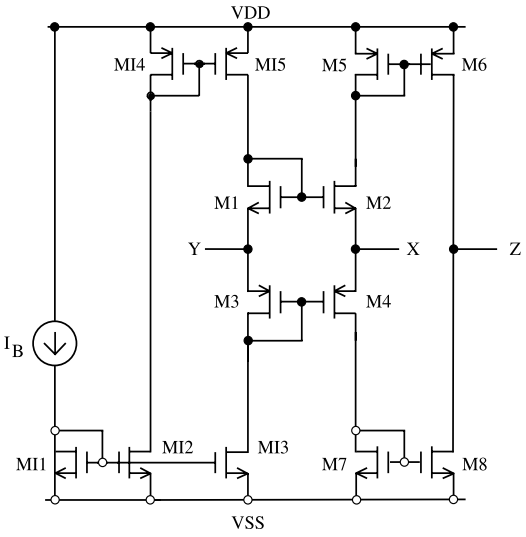
The proposed rectifier uses the CCII+ and CCII+/- circuits in Fig. 3. In the circuits the transistors M1 and M3 are used to establish the proper gate-source bias voltage for the source follower transistors M2 and M4. The small signal voltage gain from nodes Y to X [7] is given by

$$A_v = \frac{g_{m2} + g_{m4}}{g_{m2} + g_{m4} + g_{mbs2} + g_{mbs4}} \times \frac{g_{m1} + g_{m3} + g_{mbs1} + g_{mbs3}}{g_{m1} + g_{m3}} \quad \textbf{(10)}$$

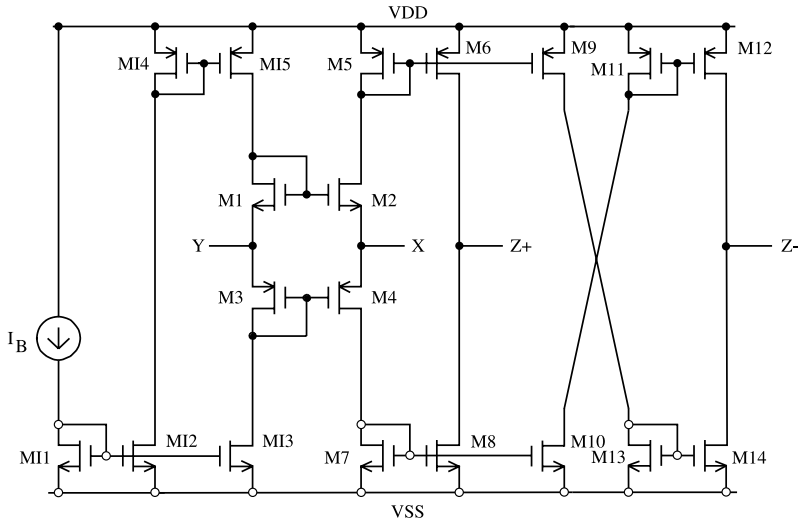
where g_{mQ} and g_{mbsQ} denote the gate transconductance and the bulk transconductance for transistor number Q, respectively. In [7], the conveyor X input impedance is also given by

$$r_x = (g_{m2} + g_{m4} + g_{mbs2} + g_{mbs4})^{-1} \quad \textbf{(11)}$$

With perfectly matched transistors (M1 matching M2 and M3 matching M4), we find A_v=1 and there is no offset voltage between nodes Y and X. A mismatch between M1 and M2 or M3 and M4 would result both in a change in A_v and in an offset voltage between nodes Y and X. By careful design, the mismatching can be limited to less than 1% and the gain error caused by a mismatch is likely to be less than 0.1%, corresponding to an input error voltage in the low millivolt range for input voltages of a few volts [7].



(a)



(b)

Fig. 3 Current conveyors used in simulation: (a) CCII+ and (b) CCII+/-.

The operation range of the proposed rectifier is limited below the supply voltage. With the same W/L ratios of M1, M2, M3, and M4, to make M2 and M4 being in the saturation mode the same as M1 and M3, the minimum and maximum input voltages that the proposed rectifier can operate are

$$\left.\begin{aligned} V_{in(\min)} &= V_{SS} + |V_{TP}| + |V_{TN}| + |V_{eff4}| + |V_{eff7}| \\ V_{in(\max)} &= V_{DD} - |V_{TP}| - |V_{TN}| - |V_{eff2}| - |V_{eff5}| \end{aligned}\right\} \quad \textbf{(12)}$$

where $V_{eff} = V_{GS} - V_T = \sqrt{\frac{2I_D}{\mu C_{OX}(W/L)}}$ [8]: V_{GS} is the gate to source voltage, V_T is the threshold voltage, I_D is the drain current, μ is the mobility of carriers, C_{OX} is the gate capacitance per unit area, W and L are the channel width and length.

3. Simulation Results

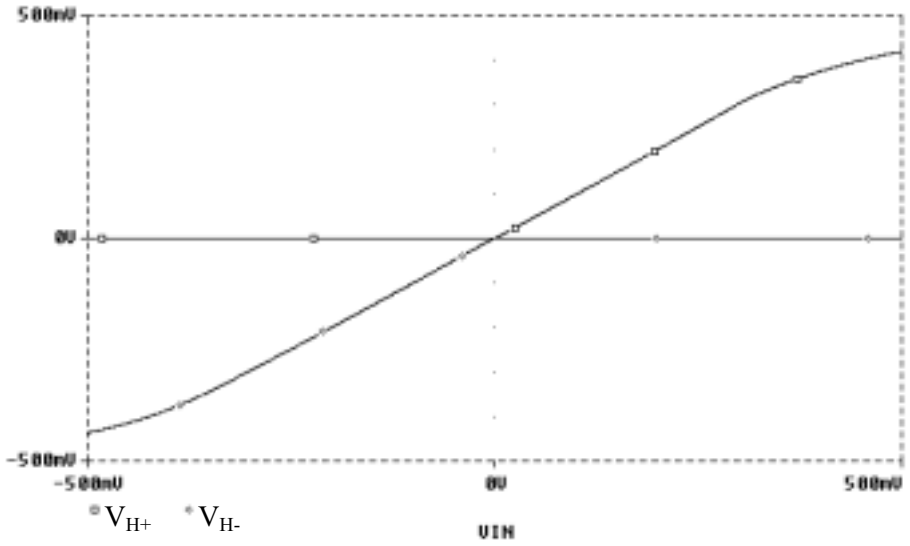
To verify a theoretical design, a proposed universal rectifier was simulated by using the PSPICE program with CMOS current conveyors fabricated in the 0.5 μm MOSFET technology from MIETEC that has a model as listed in Table 1. A diode model used in simulation is listed in Table 1 as well. Current conveyor circuits, CCII+ and CCII+/-, are shown in Fig. 3. All W/L ratios of MOSFETs in current conveyors are 20 μm / 0.6 μm. All constant current sources in current conveyors are set to 20 μA. $R_1 = R_2 = R_3 = R_4$ = 10 kΩ and $R_5 = R_6$ = 12 kΩ were chosen. Following to Eq. 9a and Eq. 9b, it shows that r_x = 2 kΩ. Note that r_x is high because the constant current sources in current conveyors are set to the low current 20 μA, in order to reduce the power consumption of the proposed rectifier. The supply voltages are ±1.2 V. The DC transfer characteristics of the proposed rectifier are shown in Fig. 4, which displays the operation voltage swing ranging from -300 mV to 300 mV of the input voltage. In this operation range, the simulated power consumption is 0.88 mW. Applying the 100 mVpeak sine wave having a frequency of 100 kHz at the input of the proposed rectifier, the input and output signals are shown in Fig. 5. It is clearly seen in Fig. 5 that the proposed universal rectifier provides high precision. The amplitude errors for different input signal voltages at some frequencies are listed in Table 2. It is evident in Table 2 that the error will be high at high frequency because of the decrease of the gain of CCIIs at high frequency.

Table 1 MOSFET and diode models used in simulation.

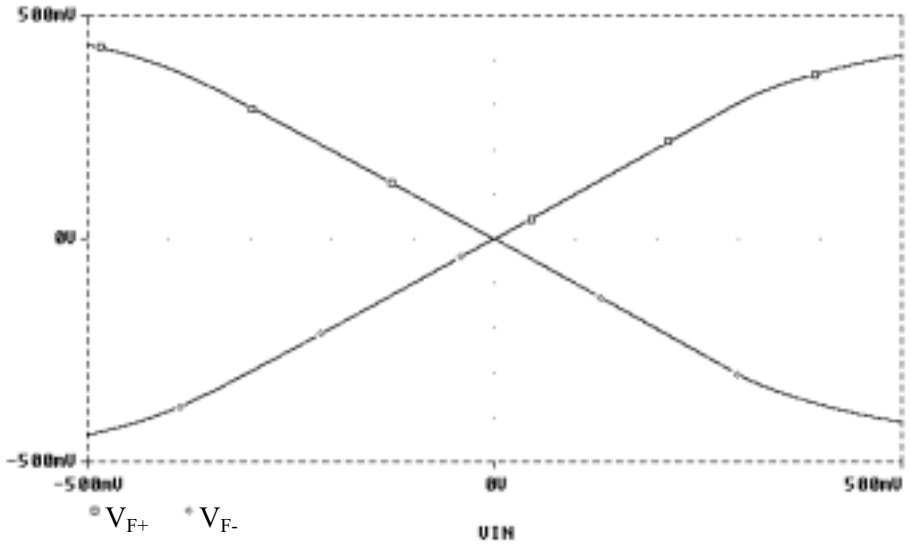
```
.MODEL NM NMOS LEVEL=3
+UO=460.5 TOX=1.0E-8 TPG=1 VTO=0.62 JS=1.08E-6
+XJ=0.15U RS=417 RSH=2.73 LD=0.04U VMAX=130E3
+NSUB=1.71E17 PB=0.761 ETA=0.00 THETA=0.129 PHI=0.905
+GAMMA=0.69 KAPPA=0.10 CJ=76.4E-5 MJ=0.357 CJSW=5.68E-10
+MJSW=0.302 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10
+KF=3.07E-28 AF=1 WD=+0.11U DELTA=+0.42 NFS=1.2E11
+DELL=0U LIS=2 ISTMP=10

.MODEL PM PMOS LEVEL=3
+UO=100 TOX=1.0E-8 TPG=1 VTO=-0.58 JS=0.38E-6
+XJ=0.10U RS=886 RSH=1.81 LD=0.03U VMAX=113E3
+NSUB=2.08E17 PB=0.911 ETA=0.00 THETA=0.120 PHI=0.905
+GAMMA=0.76 KAPPA=2 CJ=85E-5 MJ=0.429 CJSW=4.67E-10
+MJSW=0.631 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10
+KF=1.08E-29 AF=1 WD=+0.14U DELTA=0.81 NFS=0.52E11
+DELL=0U LIS=2 ISTMP=10

.MODEL D1N914 D (IS=100E-15 RS=16 BV=100 IBV=100E-15)
```

Table 2 Amplitude errors for different signal voltages at some frequencies.

Input signal (mVpeak)	Amplitude errors (%) at frequencies:				
	10 kHz	100 kHz	1 MHz	10 MHz	100 MHz
50	0.4	0.4	0.7	1.9	13.9
100	0.4	0.4	0.7	1.9	13.9
150	0.5	0.5	0.8	2	14
200	0.6	0.6	0.8	2	14.1
250	0.7	0.7	0.9	2.1	14.2
300	0.8	0.8	1	2.1	14.3



(a)



(b)

Fig. 4 DC transfer characteristics of the proposed rectifier: (a) positive and negative half-wave rectification and (b) positive and negative full-wave rectification.

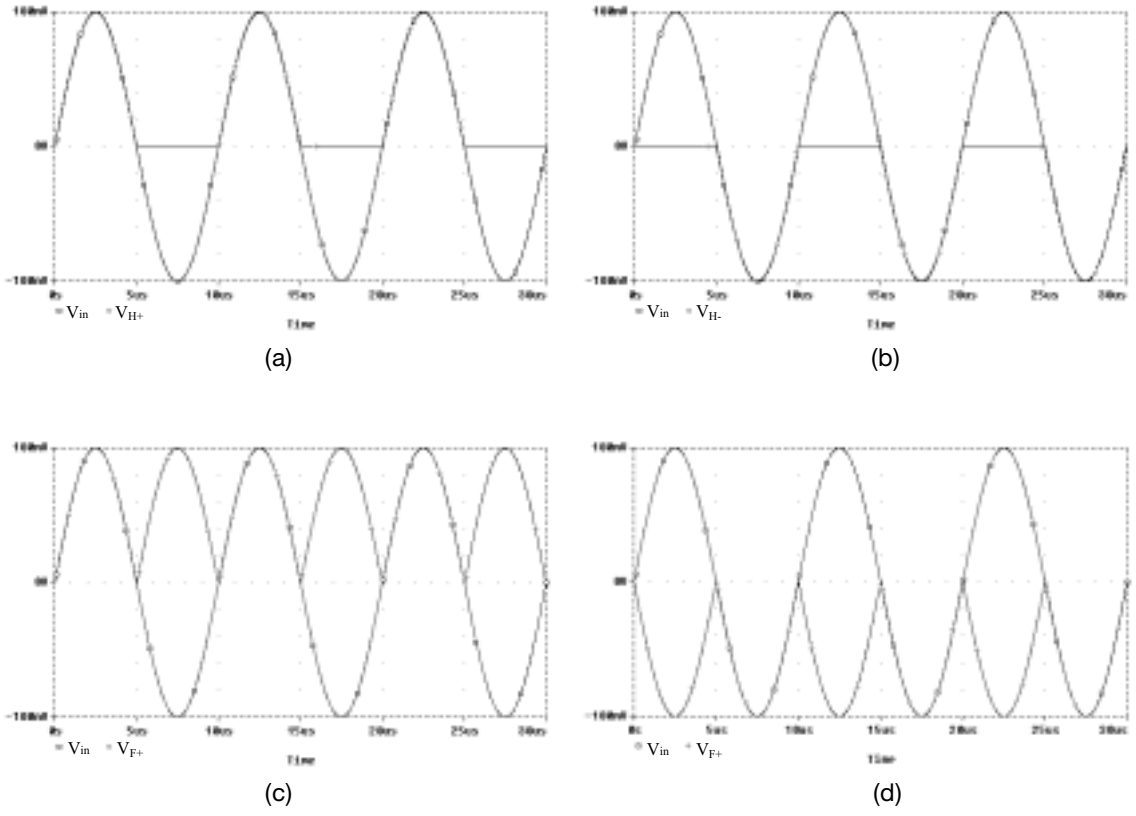


Fig. 5 Input 100 mVpeak sine wave at the frequency of 100 kHz and: (a) positive half-wave output, (b) negative half-wave output, (c) positive full-wave output, and (d) negative full-wave output.

4. Conclusion

In the paper, the authors have reported the design and simulation of a universal rectifier using current conveyors. All single-phase signal rectification can be obtained from the proposed rectifier. With current conveyors fabricated in the 0.5 μm CMOS technology from MIETEC, the proposed rectifier uses ±1.2 V supply voltages and 0.88 mW power consumption, to produce the operation voltage range from -300 mV to 300 mV. Simulation results at the frequency of 100 kHz show the high precision of the proposed rectifier. The proposed rectifier is suitable and easy to use in analog signal processing.

5. References

1. LTP Electronics Ltd., 1993, *CCII01 Current-conveyor Data Sheet,* Oxford.

2. Toumazou, C., Lidgey, F. J., and Chattong, S., 1994, "High Frequency Current Conveyor Precision Full-wave Rectifier," *Electronics Letters,* Vol. 30, pp. 745-746.

3. Hayatleh, K., Porta, S., and Lidgey, F. J., 1994, "Temperature Independent Current Conveyor Precision Rectifier," *Electronics Letters,* Vol. 30, pp. 2091-2093.

4. Khan, A. A., Abou El-Ela, M., and Al-Turaigi, M. A., 1995, "Current-mode Precision Rectification," *International Journal of Electronics,* Vol. 79, pp. 853-859.

5. Monpapassorn, A., Dejhan, K., and Cheevasuvit, F., 2001, "A Full-wave Rectifier Using a Current Conveyor and Current Mirrors," *International Journal of Electronics,* Vol. 88, pp. 751-758.

6. Sedra, A. and Smith, K. C., 1970, "A Second Generation Current Conveyor and Its Application," *I.E.E.E. Transactions on Circuit Theory,* Vol. CT-17, pp. 132-134.

7. Bruun, E., 1993, "CMOS High Speed, High Precision Current Conveyor and Current Feedback Amplifier Structures," *International Journal of Electronics,* Vol. 74, pp. 93-100.

8. Johns, D. and Martin, K., 1997, *Analog Integrated Circuit Design,* New York: John Wiley & Sons.